

The manufacturer  
may use the mark:



**Reports:**

FRS 06-11-27 R002  
FMEDA Report V1 R1  
FRS 09-10-23 R001 IEC  
61508 Functional Safety  
Assessment Report V1 R1

**Validity:**

This assessment is valid for  
the DeltaV Voltage Monitor  
Module.

This assessment is valid until  
May 11, 2013.

Revision 1.3 May 27, 2010



# Certificate / Certificat Zertifikat / 合格証

FRS 091023 C002

*exida* hereby confirms that the:

## DeltaV Voltage Monitor Module

**Emerson Process Management  
Fisher Rosemount Systems, Inc.  
Austin, TX USA**

Has been assessed per the relevant requirements of:

**IEC 61508 Parts 1, 2, 3**

and meets requirements providing a level of integrity to:

**Systematic Integrity: SIL 3 Capable  
Random Integrity for Type A Device:  
SIL 3 @ HFT=0**

**Therefore can be used as part of a safety  
instrumented system as per IEC 61511**

Safety Function:

The DeltaV Voltage Monitor Module will control its output state  
in accordance with the input signal.

Application Restrictions:

The unit must be properly designed into a Safety Instrumented  
Function per the Safety Manual requirements.



*Michael Medoff*

Product Assessor

*William M. Holt*

Auditor

FRS 091023 C002

**Systematic Integrity: SIL 3 Capable**

**Random Integrity for Type A Device:  
SIL 3 @ HFT=0**

DeltaV Voltage Monitor  
Module

Emerson Process  
Management

Austin, TX

**SIL 3 Capability:**

The product has met manufacturer design process requirements of Safety Integrity Level (SIL) 3. These are intended to achieve sufficient integrity against systematic errors of design by the manufacturer.

A Safety Instrumented Function (SIF) designed with this product must not be used at a SIL level higher than stated without "prior use" justification by end user or diverse technology redundancy in the design.

**IEC 61508 Failure Rates in FIT\***

Failure Categories	$\lambda_{sd}$	$\lambda_{su}$	$\lambda_{dd}$	$\lambda_{du}$
Voltage Monitor Module	1	134	0	0.72

**SIL Verification:**

The Safety Integrity Level (SIL) of an entire Safety Instrumented Function (SIF) must be verified via a calculation of  $PFD_{AVG}$  considering redundant architectures, proof test interval, proof test effectiveness, any automatic diagnostics, average repair time and the specific failure rates of all products included in the SIF. Each subsystem must be checked to assure compliance with minimum hardware fault tolerance (HFT) requirements.

\* FIT = 1 failure /  $10^9$  hours



Form	Version	Date
C61508	2.3	May 2010